Development of void-free focused ion beam-assisted metal deposition process for subhalf-micrometer high aspect ratio vias

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Low resistance metal deposition in deep submicron vias is required for circuit rewiring in focused ion beam (FIB)-based integrated circuit modification. Voids in high aspect ratio deposition, associated with the application of traditional FIB process to tungsten deposition in vias with aspect ratios beyond 10:1 contribute substantially to the resistance of the via. Pinch off of the via aperture is frequently observed. The dynamics of tungsten deposition within vias was studied through a series of via cross sections with variable deposition dose, and revealed accelerated deposition growth on the walls at the top of the vias. Accelerated deposition on the sidewalls, where the primary beam interacts with the substrate at a glancing angle, suggested that the deposition growth is initiated by secondary charged particles generated at the point of primary beam impact rather than by the primary beam itself. The results are in agreement with mechanisms previously proposed and confirmed by experiments. In order to prevent the generation of secondary particles on the walls of the via, and the consequent pinch off closure of the via aperture, confining the primary beam to an area much smaller than the aperture of the via was attempted. With this process, secondary particles are generated at the bottom of the via and trapped within the via, which was expected to lead to bottom-up deposition growth. A dose series study of the deposition produced by the proposed process confirmed the uniform growth of the tungsten fill from the bottom of the via. Void-free depositions were made in 5 μm deep vias ranging in size from 0.5 μm by 0.5 μm to 0.2 μm by 0.2 μm, corresponding to aspect ratios from 10:1 to 25:1, respectively. [DOI: 10.1116/1.1621666]

I. INTRODUCTION

Filling high aspect ratio (HAR) vias by focused ion beam (FIB) deposition frequently results in incomplete via fill (Fig. 1) with large voids in material deposited within the via. Recommendations for achieving good via fill with a FIB[1–4] have consistently advised "staying away" from via walls, as typical via aspect ratios increased beyond 1.5:1. Recent dramatic increases in the aspect ratios needed to access the internal nodes of modern integrated circuits, required better understanding of via fill process and improved deposition strategy.

The main models[5–8] proposed over the last decades to explain the FIB deposition mechanism, are based either on secondary electron interaction or on ion cascade principles. Work of Lipp *et al.* demonstrated a link between secondary electron yield and deposition rate for both electron beam and ion beam induced deposition processes. Both types of models predict enhanced deposition rates at glancing angles of ion beam incidence in agreement with experiment,[3,6] where sputtering rates are also higher.

Based on the assumption of possible effective deposition of material, induced by the secondary particles generated from the primary ion beam interaction within the via, it was proposed to confine the ion beam during deposition process to an area much smaller, than the size of the via. Interactions between the ion beam and the via sidewalls would thereby be minimized by physical separation between the via walls and the ion beam. Most of the secondary particles, generated at the bottom of the HAR via, would be trapped within the via due to "Faraday cup" effect. Low energy secondary particles, generated at the bottom of the HAR via, are more likely to be absorbed on the sidewalls than to escape the via. Therefore the deposition, induced by the ion beam confined to area much smaller than the size of the via, is expected to grow from the bottom to the top of the via and result in void-free via fill.

Deposition in HAR vias differs from the deposition on the surface in that there is slower replenishment of deposition

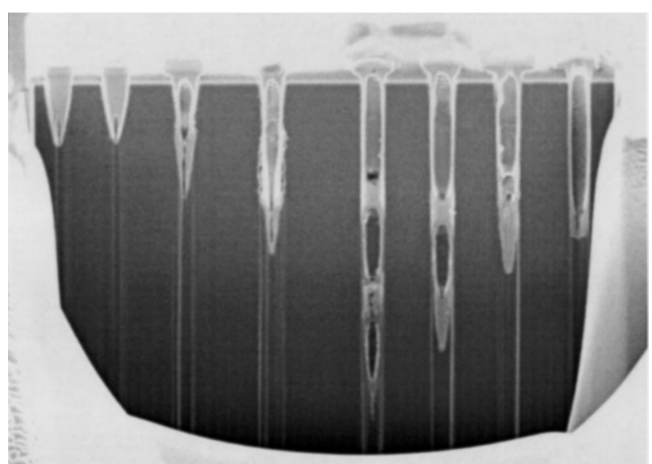

FIG. 1. Cross-sectional image of series of 0.5 μm×0.5 μm vias with depth ranging from ~3 to ~10 μm, filled with tungsten by the 0.35 μm×0.35 μm deposition box, shows formation of large deposition voids in HAR vias.

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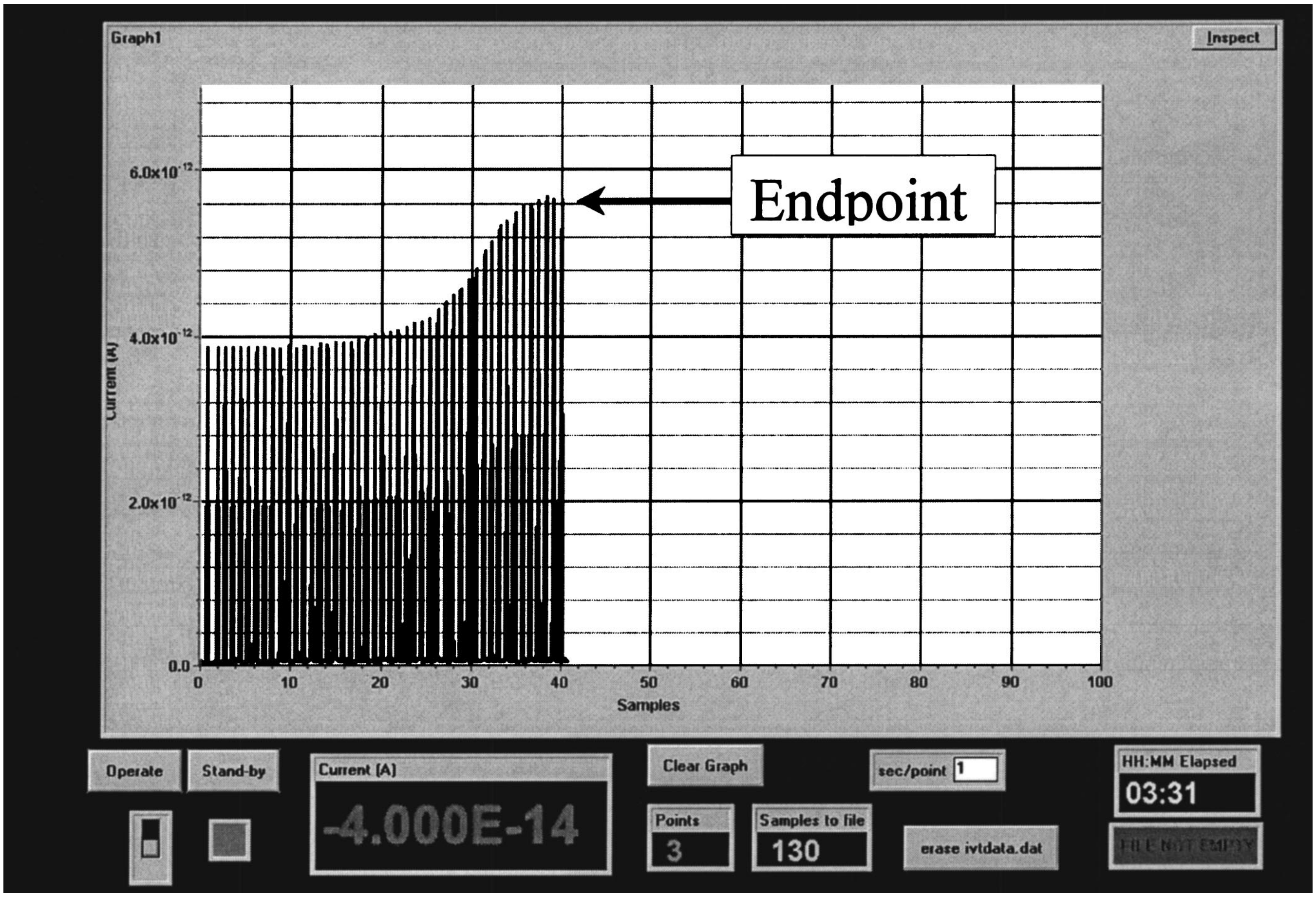

FIG. 2. Main screen of experimental TESTPOINT data plotting application with the typical shape of the plot observed on the sample absorbed current monitoring setup at the endpoint of the via fill deposition. *X* axis represents consequent current sample number in arbitrary units.

precursor due to the low gas flow conductance of the via. Using high beam currents for HAR via fill would result in fast gas depletion and possible milling (rather than deposition) at the bottom of the via. We successfully used low beam current deposition as an alternative approach for HAR via fill.

II. EXPERIMENTAL DETAILS

A series of via fill experiments was conducted on an FEI VectraVision Circuit Edit tool. This tool is equipped with the VisION ion column based on liquid metal ion source (LMIS). We did not measure the actual beam size during via fill experiments.

Primary ion beam current was adjusted to the 5 pA value by selecting the 15 μm beam limiting aperture. The current was measured by *in situ* ion Faraday cup and controlled periodically to ensure stability within 10% of the set value during the experiments. The beam was rastered within the deposition box area in a serpentine pattern.

Tungsten hexacarbonyl gas was used as a deposition precursor. It was delivered by the gas delivery nozzle, extended from a heated crucible reservoir to release the gas in close proximity of the via. Pressure in the system chamber was increasing from base level of $2.8E\text{-}7$ to $6.2E\text{-}6$ Torr when the deposition precursor was released.

Low aspect ratio [(LAR)<5:1] vias, 0.5 μm$\times$0.5 μm and 1.5 μm deep, were milled in a Si substrate and filled by various doses of ion beam exposure within a 0.6 μm$\times$0.6 μm deposition box in the presence of tungsten hexacarbonyl precursor. The test allowed verification of the effects of ion beam induced deposition on via sidewalls.

In an effort to avoid the interaction between the ion beam and via sidewalls while filling HAR vias, we used manual position correction techniques to compensate for the drift naturally present in a FIB system. The position correction allowed to compensate for system drifts and ensure the deposition was always centered on the via.

HAR (5:1<HAR<10:1) vias, 0.4 μm$\times$0.4 μm and 2.4 μm deep, were milled in a Si substrate and filled with tungsten by various doses of ion beam exposure within 0.1 μm $\times$0.1 μm deposition box in the presence of tungsten hexacarbonyl precursor to evaluate proposed via fill approach.

Filling ultra high aspect ratio [(UHAR)>10:1] vias, 0.5 μm$\times$0.5 μm and deeper than 20 μm was also attempted by ion beam exposure within the 0.15 μm$\times$0.15 μm deposition box in the presence of tungsten hexacarbonyl precursor.

All vias, milled in Si, were covered by a dielectric cap

FIG. 3. Cross-sectional image of 1.5 μm deep 0.5 μm$\times$0.5 μm LAR vias, filled with tungsten by the 0.6 μm$\times$0.6 μm deposition box. Large voids within the deposited material are the indication of incomplete via fill.

deposited by a 0.75 μm$\times$0.75 μm deposition box, in order to preserve the details of the via filling process in incompletely filled vias prior to cross sectioning the via for analysis.

The proposed via filling technique was also applied to filling a series of HAR and UHAR vias in SiO_2 dielectric. The series of 5 μm deep vias with sizes ranging from 0.5 μm$\times$0.5 μm down to 0.15 μm$\times$0.15 μm were filled by ion beam exposure within the deposition box with size 1/4 from the size of the via being filled. For example, the 0.1 μm$\times$0.1 μm deposition box was used for filling the 0.4 μm$\times$0.4 μm via.

We developed and evaluated a via fill control technique, based on monitoring the sample-absorbed current flowing from the sample bombarded by an ion beam to the grounded stage of the FIB system. During the bottom-up deposition growth within the via the aspect ratio of unfilled portion of the via is gradually decreasing. Therefore the probability of escaping for the secondary particles, both electrons and ions, generated within the via, increases and the sample-absorbed current should increase also. Once the via is filled completely, all of the secondary particles are generated at the surface level and therefore the sample absorbed current should not undergo any further changes.

III. RESULTS AND DISCUSSION

An experimental setup for evaluating the proposed via fill control technique was based on the Keithley 6487 picoammeter with low noise and subPico ampere resolution. Input of the picoammeter was routed into the vacuum chamber of the FIB system through the coaxial vacuum feedthrough. The sample holder, with the sample mounted on it, was electrically isolated from the ground and the picoammeter was connected by coaxial cable between the sample holder and the grounded stage of the FIB system. Current measurement data were transferred from the picoammeter to a computer through digital interface and visualized by a data plotting application created in TESTPOINT software. This setup allowed detecting distinct variations of the sample-absorbed current and defining the endpoint of the via fill at the time

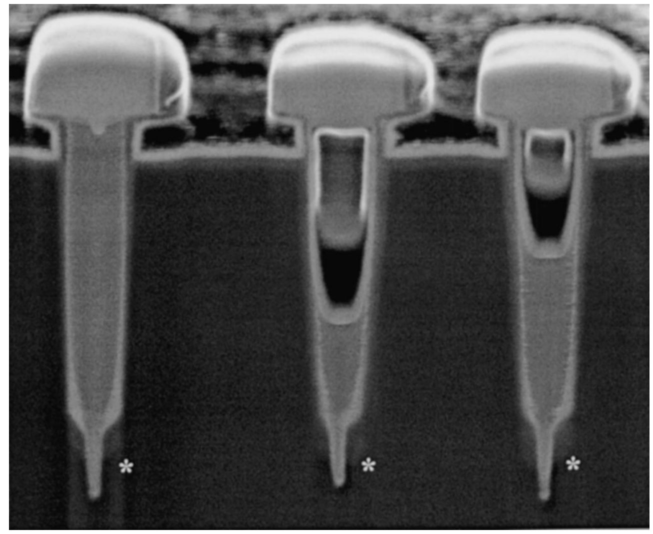

FIG. 4. Cross-sectional image of 2.4 μm deep 0.4 μm$\times$0.4 μm HAR vias, gradually filled with tungsten by the 0.1 μm$\times$0.1 μm deposition box. The small tip at the bottom of the vias was caused by precursor gas depletion and milling by relatively high ion beam current during deposition.

when the deposition approached the surface of the sample. Reliable endpoint detection (Fig. 2) was possible for the via fill deposition process.

Cross sections of 1.5 μm deep 0.5 μm$\times$0.5 μm LAR vias, filled with tungsten by 0.6 μm$\times$0.6 μm deposition box (Fig. 3) revealed fast growth of the metal on via sidewalls at the top of the via. It is interesting to note that even at these low aspect ratios metal deposition on the bottom of the via was minimal and the via fill had large voids within the FIB deposited tungsten.

A cross-sectional image of 2.4 μm deep 0.4 μm$\times$0.4 μm HAR vias (Fig. 4), filled with tungsten by a 0.1 μm$\times$0.1 μm deposition box, showed gradual growth of metal deposition and filling of the via from the bottom up. The leftmost via on Fig. 3 was filled completely and the dose of the ion beam exposure, at which filling finished, was recorded. The middle via was filled with 1/3 of the recorded ion beam dose and the rightmost via filled with 2/3 of the dose.

A small tip, protruding down from the floor of the via into the bulk Si substrate, was observed on all HAR vias. Milling of the substrate, caused by excessive beam current during the deposition process, is an apparent cause of the tip formation.

Metal deposition in deeper than 20 μm 0.5 μm$\times$0.5 μm UHAR vias started to grow from the bottom of the via [Fig. 5(a)]. However filling was not completed due to pinch off of the via aperture [Fig. 5(b)]. We attributed this to inefficiencies of the manual beam placement control technique and to the enhanced deposition of the metal at the edge of the via during imaging with the precursor gas present. Short, but relatively frequent, interactions between the ion beam and the via sidewalls in the proximity of the via aperture caused accelerated growth of deposition and eventual pinch off of the via aperture.

The series of 5 μm deep vias, milled in SiO_2 dielectric and filled with tungsten by ion beam exposure within the

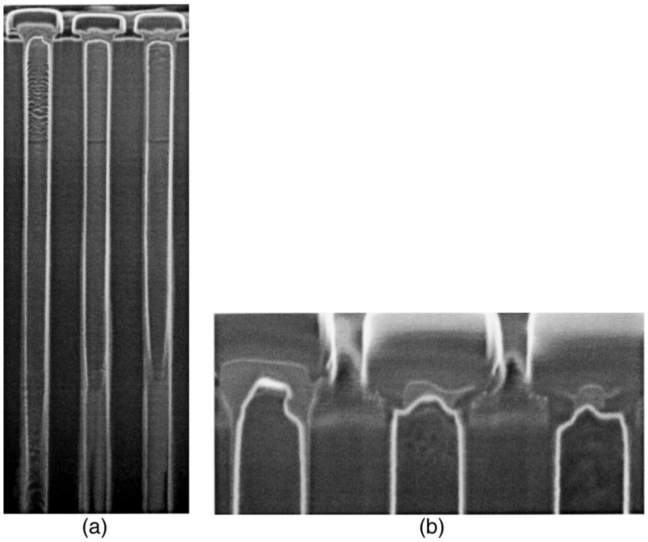

FIG. 5. Cross-sectional image of 0.5 μm$\times$0.5 μm UHAR vias with $>$40:1 aspect ratio, showing bottom-up fill by 0.15 μm$\times$0.15 μm deposition at the beginning of the deposition (a) and interruption of the filling process due to closing of via aperture (b).

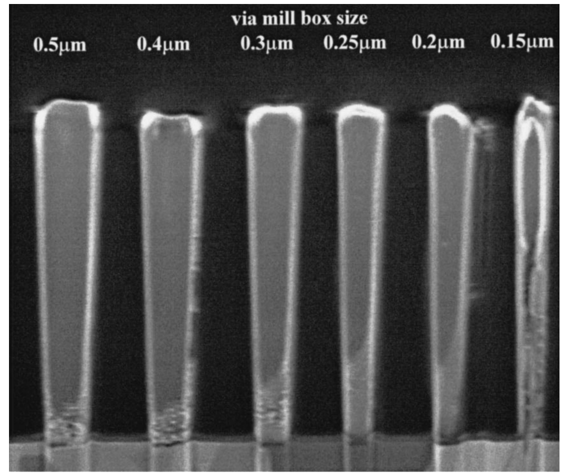

FIG. 6. Cross-sectional image of the series of 5 μm deep vias milled by FIB in SiO_2 dielectric substrate and filled void free with tungsten by deposition boxes measured 1/4 of the via size for vias with aspect ratio in range from 10:1 (0.5 μm$\times$0.5 μm) to 25:1 (0.2 μm$\times$0.2 μm), based on via mill box size.

deposition box with size 1/4 from the size of the via being filled demonstrated successful void-free fill of the vias from 0.5 down to 0.2 μm (Fig. 6). In the case of the 0.15 μm via, pinch off occurred before the filling process was completed.

IV. IMPLICATIONS FOR FIB DESIGN AND USE

A few potential enhancements of the FIB system may be proposed to overcome observed difficulties with filling UHAR vias. Ultralow beam currents ($\leqslant$1 pA) could be used to avoid precursor gas depletion during deposition at the bottom of the HAR and UHAR vias. Lower beam currents would allow further reduction of the ion beam spot size. Automated beam placement control through pattern recognition could improve the efficiency of the drift compensation. Elimination of the beam blanking during via deposition may improve the graph of the sample-absorbed current and help maintain process steady-state conditions. There is a potential possibility to improve precursor gas refresh by using advanced rastering techniques, like interlaced raster, interlaced scrpentine, or other Lissajous-like patterns with increased built-in refresh periods. Sample absorbed current monitoring has the potential for automating via fill control.

With the general tendency of reducing dimensions of the internal features of integrated circuits, we expect to see a growing demand of the circuit debug industry to mill and effectively fill even smaller vias. Since the cross-sectoinal area of the via reduces as the square of the via diameter, demand for good quality via filling would increase significantly.

It has been reported in the literature that electron beam induced deposition of metals and dielectric materials is possible. Absence of gallium implantation in e-beam deposited dielectric and, as reported by Ochiai *et al.*,[9] possibility of highly conductive e-beam induced metal deposition, could be attractive for in-via fill. Nonetheless e-beam induced deposition rates[9,10] are relatively low in comparison with the typical deposition rates for the ion beam induced process, the e-beam induced deposition could be viable for filling vias on the scale below 50 nm.

V. FUTURE WORK

Resistivity of the conductor, formed by the in-via metal fill, is a critical parameter of the via fill deposition in focused particle beam based integrated circuit (IC) modification. Influence of the local pressure of deposition precursor at the via opening, ion beam current, and raster parameters, along with the chemical composition of the deposited material should be studied and optimized.

Differences in chemical composition of the deposited metal between the in-via area, directly affected by the ion beam during the deposition process, and periphery of the via could be investigated in order to gain better understanding of the via fill process.

Detailed evaluation of the feasibility of via filling by the electron beam induced deposition process could be of much interest for future developments.

VI. CONCLUSION

A deposition strategy for filling deep submicron HAR access vias in modern IC modification and debug FIB tools was proposed and experimentally evaluated. The proposed deposition technique produces void-free metal deposition in HAR and UHAR vias in Si and SiO_2 substrates.

Via fill endpoint detection technique, based on monitoring the sample absorbed current, was proposed and demonstrated experimentally.

Factors, limiting the void-free deposition in UHAR vias and vias smaller than 0.15 μm, were identified and technological approaches were proposed to achieve void-free filling of such vias.

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