

Sample Preparation for Backside Circuit Modification (Backside FIB Circuit Edit)  
Abbreviated\* Application Training Syllabus.

1. Types of microelectronics packaging and decapsulation methods
2. Substrate thickness and surface quality requirements for backside FIB Circuit Edit
3. Lapping and flat polishing
4. Fuming acid decapsulation
5. CNC decapsulation
6. Combined decapsulation methods
7. Substrate thinning process
8. Surface polishing process
9. Typical defects of sample preparation
10. Tools and accessories

\*Detailed syllabus is available upon request sent to: [info@partbeamsystech.com](mailto:info@partbeamsystech.com)